

Electrochemically controlled transport of lithium through ultrathin SiO₂

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Monolithically integrating the energy supply unit on a silicon integrated circuit (IC) requires the development of a thin-film solid-state battery compatible with silicon IC fabrication methods, materials, and performance. We have envisioned materials that can be processed in a silicon fabrication environment, thus bringing local stored energy to silicon ICs. By incorporating the material directly onto the silicon wafer, the economic parallelism that silicon complementary metal-oxide-semiconductor (CMOS) technology has enjoyed can be brought to power incorporation in each IC on a processed wafer. It is natural to look first towards silicon CMOS materials, and ask which materials need enhancement, which need replacement, and which can be used “as is.” In this study, we begin by using two existing CMOS materials and one unconventional material for the construction of a source of electric power. We have explored the use of thermally grown silicon dioxide (SiO₂) as thin as 9 nm acting as an electrolyte material candidate in a solid-state power cell integrated on silicon. Other components of the thin-film cell consisted of rf-sputtered lithium cobalt oxide (LiCoO₂) as the cathode and highly doped *n*-type polycrystalline silicon (polysilicon) grown by low-pressure chemical-vapor deposition as the anode. All structures were fabricated using conventional microelectronics fabrication technology. The charge and discharge behaviors of the LiCoO₂/SiO₂/polysilicon cells were studied. On the basis of the impedance measurements an equivalent circuit model of an ultrathin cell was inferred, and its microstructure was characterized by electron microscopy imaging. In spite of its high series resistance ($\sim 4 \times 10^7 \Omega$), we have shown that an ultrathin layer of an as-deposited Li-free SiO₂ is an interesting candidate for an electrolyte or controllable barrier layer in lithium-ion-based devices. © 2005 American Institute of Physics. [DOI: 10.1063/1.1989431]

INTRODUCTION

Silicon complementary metal-oxide semiconductor (CMOS) technology has advanced significantly by implementing integration of various electronic circuit elements onto a single chip. Examples of the successful integration of various electronic and optoelectronic components with silicon integrated circuits (ICs) include germanium *p*-type metal-oxide semiconductor field-effect transistors (*p*-MOSFETs),¹ silicon germanium on insulator (SGOI) for high-speed and low-power applications,² optical links of GaAs *p-i-n* light-emitting diode (LED) and detector diodes,³ as well as Al_xGa_{1-x}As/In_xGa_{1-x}As LEDs and lasers.⁴ It is natural to consider what system-level function may be integrated next onto the silicon CMOS platform. One important remaining integration challenge is to incorporate the energy source, initially as part of the global power supply, onto the silicon chip. This requires the development of a thin-film solid-state battery, compatible with silicon IC technology in terms of fabrication methods, materials, and performance. The low-power requirements of CMOS-technology-based devices make it possible to consider the design of electrical energy storage devices composed of materials compatible with microelectronic technology but unlikely choices in conventional batteries. Subsequently, higher power or voltage

requirements might be met through the use of a multilayered structure, in which the power cells are connected in parallel or in series, respectively.

One of these materials, a most commonly used and well-studied material in silicon IC technology, is silicon dioxide (SiO₂). SiO₂ is used as an insulating field material between devices, as an intermetal dielectric material, and as a transistor gate dielectric layer. It is a chemically stable material, with an energy gap E_g of ~ 8 eV, electronically insulating, and known to be susceptible to the diffusion of alkali-metal cations. An interesting aspect of incorporating solid-state power sources on semiconductors is that light ion motion in oxides is well known in the MOSFET world, since this was a main barrier to commercialization of MOSFET devices. The insulating properties of SiO₂, its permeability to light cations, and the high degree of process control available in the generation of thin SiO₂ layers, which is a result of microelectronic advances, have motivated us to investigate the use of SiO₂ as a solid-state electrolyte in our integrated thin-film lithium-ion power cell. The risk of device contamination by lithium diffusion can be eliminated by implementing the battery fabrication into the back-end processes which occur after the die is finished. Furthermore, the battery can be fabricated in a separate area from the chip itself, prior to the wafer slicing, chip wiring, and packaging which are included in the back-end process. Such integration of a device containing a potentially contaminating element is similar in some sense to the successful integration of copper intercon-

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nects in CMOS technology. Common solid-state electrolytes currently in use consist of a lithium-containing or lithium-doped electronically insulating material, typically 1–2 μm thick. Examples include lithium phosphorus oxynitride (LiPON),^{5–7} polymers doped with lithium salts,⁸ and various types of lithium-containing oxide glasses.^{9–11} Hence, SiO_2 is an unconventional electrolyte because even when undoped with lithium salt the material appears to facilitate the diffusion of Li^+ . One might expect that a material that does not inherently contain lithium ions would become positively charged upon ingress of Li^+ ions, thereby creating an electric field that would halt the diffusion. However, we show here by using microelectronic processing expertise that the SiO_2 electrolyte can be created sufficiently thin to allow rapid diffusion of lithium ions through it. Kushida *et al.*¹² studied a porous glassy SiO_2 –15 at. % P_2O_5 electrolyte 0.5–1.5 μm thick, in which diffusion of lithium ions occurred via fast paths on the pores' surface. We report the study of controlled transport of lithium through an ultrathin lithium-free as-deposited SiO_2 film, 9–40 nm thick. The SiO_2 is grown by thermal oxidation of a polycrystalline silicon (polysilicon) layer, which serves as the anode or negative electrode of our power cell. The use of heavily doped polysilicon as an electrode is highly advantageous from a processing perspective, since its formation can be readily integrated into conventional microdevice fabrication processes. The lithium-silicon system has been a subject of numerous studies due to silicon's high theoretical capacity of up to 1967 mA h/g for $\text{Li}_{21}\text{Si}_5$ (Ref. 13) and lithium's high diffusivity in silicon of $D_{\text{Li}} \sim (2\text{--}3.5) \times 10^{-14}$ cm^2/s (Ref. 14) at room temperature. One potential problem with using silicon as an electrode is the fact that the chemical reaction between silicon and lithium involves significant volume changes due to the reduced density of the silicon-lithium compounds compared to that of silicon. Using a thin film of polysilicon might alleviate this problem, thanks to the higher ratio of surface area to volume and thanks to its grain boundaries. The cathode in our thin-film power cell stack is a nanocrystalline layer of LiCoO_2 . The $\text{LiCoO}_2/\text{SiO}_2/\text{polysilicon}$ cells were fabricated and patterned using conventional microelectronics processing. This study introduces SiO_2 as a candidate electrolyte for battery applications and demonstrates its performance as deposited lithium-free in a lithium-ion power cell. We reason that, in addition, the controlled ion transport observed in this material can potentially be used in other interesting electronic or optoelectronic devices.

EXPERIMENTAL PROCEDURE

The integrated power cells, up to the electrolyte layer, were created in a class 10 clean room on an insulating layer grown on a (100) silicon substrate. In principle, the method described here could allow an integrated battery to be grown on the backside of the wafer as part of the back-end silicon processing on the chip. A 300-nm-thick polysilicon anode layer was grown by low-pressure chemical-vapor deposition (LPCVD) at 625 $^\circ\text{C}$ from a SiH_4 gas precursor and was highly doped *in situ* with phosphorus to make it electronically conductive (*n*-type). SiO_2 films grown directly from

doped polysilicon were not electronically insulating due to phosphorous diffusion which occurred during oxidation. Therefore, in order to obtain better quality of SiO_2 and to maintain better control over thickness and uniformity, a thin layer (14 nm) of undoped polysilicon layer was deposited at 550 $^\circ\text{C}$ on top of the doped polysilicon. The undoped polysilicon layer was subsequently partially oxidized at 700 $^\circ\text{C}$ to create a uniform layer of SiO_2 on top of the residual lower part of the undoped polysilicon layer to which phosphorus may have diffused during oxidation. SiO_2 films grown under these conditions are entirely amorphous and were tested to be electronically insulating. In this work two thicknesses of SiO_2 were evaluated, 9 and 40 nm. rf sputtering in an argon ambient was used to deposit the LiCoO_2 cathode layer at 200 $^\circ\text{C}$ from a commercially purchased LiCoO_2 target. The thickness of the deposited LiCoO_2 films was 250 nm. By transmission electron microscopy (TEM) imaging and electron diffraction the films were determined to be polycrystalline. Secondary-ion-mass spectrometry (SIMS) determined the Li:Co ratio in the as-deposited films to be 0.7. Electrode contacts (current collectors in battery terminology) were made of bilayers of titanium and aluminum, with titanium contacting the electrode. The cathode contact was deposited by sputtering and the anode contact was formed by electron-beam evaporation. The wafer was patterned using photolithography and a wet chemical etch to create square cells of three different sizes with active areas measuring 5×5 , 2×2 , and $1 \times 1 \text{mm}^2$ and fitted with a "body type" square ring back contact to minimize resistance and to allow contacting both cathode and anode from the same side of the wafer. The aluminum layer was etched at 50 $^\circ\text{C}$ employing a commercial aluminum etching solution, type A, consisting of $\text{H}_3\text{PO}_4:\text{HNO}_3:\text{HAc}:\text{H}_2\text{O}$ (16:1:1:2). The titanium and LiCoO_2 etches were performed with a solution of $\text{HF}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (1:1:20). The fabricated cells were electronically isolated from each other by etching trenches inside the polysilicon layer using a chemical etch of $\text{HNO}_3:\text{H}_2\text{O}:\text{NH}_4\text{F}$ (126:60:5). The deposited and patterned cells were annealed for 1 h at 400 $^\circ\text{C}$ in N_2 in order to improve the quality of the contacts and the LiCoO_2 film.

The microstructure of the layers was studied by a cross-section high-resolution transmission electron microscopy (XHRTEM) using a JEOL 2010-FX instrument operated at 200 kV. The cell surfaces were observed by environmental scanning electron microscopy (SEM) using a Philips/FEI XL30 field-emission gun environmental scanning electron microscopy (FEG-ESEM). Producing thin-film batteries using silicon fabrication methods enables the production of very small cells as described above. In addition, such small cells can be characterized with conventional microelectronic testing equipment. Electrical measurements (to study the cell's behavior in the course of charging and discharging) were performed with a HP 4256C parameter analyzer and a probe station while contacting the cell leads with 10- μm diameter probe tips. Such apparatus is not designed to be utilized for the long testing times customary in conventional battery cycle testing; therefore, in this work, we were forced to constrain our total charge and discharge times. Moreover, the charge and discharge were not limited to a voltage range

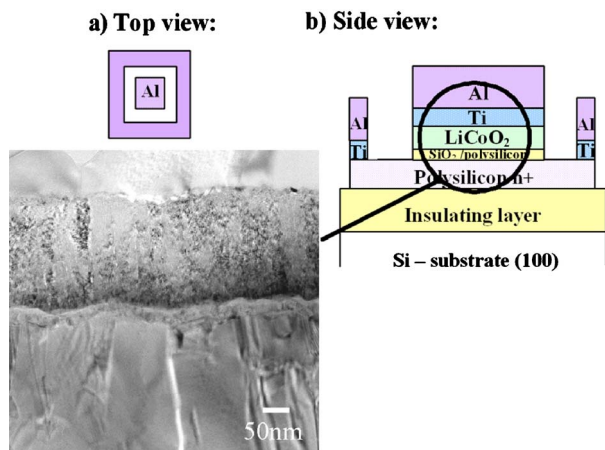


FIG. 1. A schematic description of the deposited cell, (a) top view and (b) side view, and a XHRTEM picture of a $\text{LiCoO}_2/\text{SiO}_2/\text{polysilicon}$ stack with a 9-nm-thick oxide on a 14-nm undoped polysilicon layer.

in order to learn more about the system's behavior. Impedance measurements were performed with a Solartron 1255 frequency response analyzer applying an ac voltage signal of 100 mV and measuring the current response over the frequency range of 1– 10^5 Hz. The equivalent circuit was constructed and fitted to the measured values of impedance with the aid of the ZVIEW software by Scribner Associates.

RESULTS AND DISCUSSION

Shown in Fig. 1 is a schematic representation of the integrated $\text{LiCoO}_2/\text{SiO}_2/\text{polysilicon}$ power cell, (a) top view and (b) side view. The thicknesses of the layers are not to scale. The XHRTEM image in the inset of Fig. 1 shows a 9-nm SiO_2 thick layer (on top of a residual undoped polysilicon layer) lying between the polysilicon layer (below) and the LiCoO_2 (above) contained in the cell. It is evident in the XHRTEM image in Fig. 1 that the films are continuous and bounded by high-quality interfaces between the layers. LiCoO_2 is a commonly used cathode material with a theoretical capacity of ~ 145 mA h/g for the extraction of 0.5 Li. Its crystallographic structure is hexagonal in which the oxygen anions form a closed-packed network with the lithium and cobalt cations on the alternating (111) planes of the cubic rocksalt sublattice.

The cells in this study were fabricated in their discharged state, in which lithium is intercalated in the CoO_2 host lattice. If SiO_2 behaves as an electrolyte, it should be possible to transport lithium in the form of the cation, Li^+ , from the Li_xCoO_2 cathode to the polysilicon anode by the action of electric current, which results in charging of the cell. Furthermore, after the cell has been charged, demonstrating the ability to draw current from it would be another confirmation that the SiO_2 is acting as an electrolyte wherein the charge carriers are lithium ions. Shown in Fig. 2 are the results of galvanostatic charging and discharging of different sizes of cells which were all conducted at values of current that would charge or discharge the cell in 4 h, i.e., corresponding to a so-called C rate of 0.25C.

Charging the cell forces deintercalation of Li^+ out of the positively charged LiCoO_2 host with attendant shift in va-

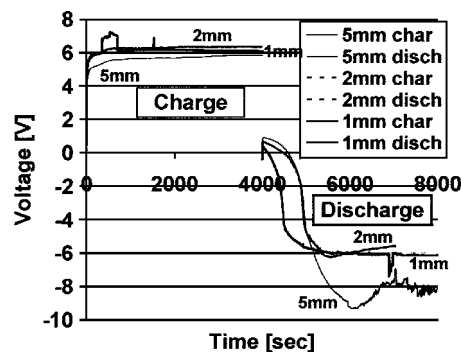


FIG. 2. Charge and discharge behavior at 0.25C of cells of different sizes with a 9-nm-thick SiO_2 electrolyte.

lence of cobalt from 3+ to 4+ along with release of one electron to the external circuit. The lithium ions diffuse across the thin SiO_2 layer to the negatively charged polysilicon electrode. At the $\text{SiO}_2/\text{polysilicon}$ interface electron transfer occurs, resulting in the reduction of Li^+ to neutral elemental lithium which chemically reacts with the host polysilicon to form one of four Li–Si compounds: $\text{Li}_{12}\text{Si}_7$, Li_7Si_3 , $\text{Li}_{13}\text{Si}_4$, or $\text{Li}_{21}\text{Si}_5$. As the cell charges, the difference in the chemical potential of lithium between the electrodes increases, which is reflected in the increase in the measured voltage as can be seen in Fig. 2. The open-circuit voltage (OCV) between elemental silicon and elemental lithium has been measured to be ~ 1 V (Refs. 15 and 16) and found to be dependent on silicon morphology.¹⁷ The OCV between Li_xCoO_2 and elemental lithium is ~ 3.5 –4 V (Refs. 7 and 18–21) depending on the lithium concentration in Li_xCoO_2 and film morphology. Combining these values, we estimate the equilibrium voltage between the electrodes in our cell to be ~ 2.5 –3 V, a value that should increase upon charging. The greater values reported in Fig. 2 reflect the high series resistance of our cells, R_s , as well as other reaction and kinetic barriers, η (polarization in battery terminology):

$$V_{\text{measured}} = V_{\text{OCV}} + IR_s + \eta, \quad (1)$$

where I represents the cell current.

Discharging the cell is accomplished by a constant current from the cells into the parameter analyzer. The current flowing in that direction is defined by the instrument as negative. Upon discharge, the lithium-silicon compounds which are believed to form during charging decompose; neutral lithium so released is oxidized to Li^+ , and the lithium ions are transported across the SiO_2 to the LiCoO_2 electrode into which they intercalate at which point Co^{+4} converts to Co^{+3} . The latter is accomplished by the consumption of electrons which are generated at the anode and furnished via the external circuit. The IR_s drop in this case is negative because of the polarity assigned by the parameter analyzer for this direction of current. The discharge is characterized by a decreasing potential difference, V_{OCV} . In our tests, we did not restrict the voltage range. Therefore, when V_{OCV} decreases beyond the point where in Eq. (1) $V_{\text{measured}}=0$ and $V_{\text{OCV}} + \eta = IR_s$, the polarity of the voltage will change. The unlimited voltage range combined with the assignment of polarity by the instrumentation accounts for the apparent negative poten-

tials seen in Fig. 2. In the initial stage of the discharge process, the right side of Fig. 2, where voltage is decreasing with time, the voltage values are lower for smaller cell sizes compared to larger cells. This voltage difference is due to the fact that there is a higher number of Li^+ available in the larger-area cell, which contains a larger volume of lithium ions, leading initially to higher current from the electrochemical process. Therefore less voltage is required by the parameter analyzer to drive the constant current in this experiment. However, as the discharge process proceeds beyond ~ 6000 s, the correlation of discharge voltage to area size is now inverted. Recall that our device geometry requires a lateral bottom contact (Fig. 1), and therefore when the device area gets large, a large series resistance will exist between the outer anode ring contact and the center of the larger area. A large voltage will therefore be needed to extract lithium ions from the center of the device. Another thing to note is that the duration of the initially positive stage of the voltage is longer for larger active area cells due to a larger volume containing a higher number of charge carriers. Since the charging voltage is increased by the series resistance and the discharging voltage is decreased by the series resistance, the overall cell resistance can be estimated by half of the difference between the end value of the charging voltage and the starting discharging voltage for the different sizes of cells. The estimated cell resistance values are $\sim 4.25 \times 10^6$, $\sim 2.85 \times 10^7$, and $\sim 1 \times 10^8 \Omega$ for the 5-, 2-, and 1-mm square edge cells, respectively. We have to keep in mind that at the initial stage of the discharge, the lateral series resistance is less dominant and more lithium ions are available at larger cells, leading to higher positive voltage and lower cell resistance in this evaluation. Moreover, this estimation does not take into account kinetic barriers, which scale inversely with lithium-ion concentration. Measuring positive voltage while drawing current from the $\text{LiCoO}_2/\text{SiO}_2/\text{polysilicon}$ cell is a clear indication of power delivery upon discharging. These measurements are consistent with the hypothesis that a thin layer of lithium-free SiO_2 can function as an electrolyte in an electrochemical energy storage device.

In order to examine the effect of charge/discharge rate on the cells, the cells were tested at different rates ranging from 0.1C to 1C which represent current densities corresponding to drain times of from 10 to 1 h, respectively. Additionally, in order to test the cells in extreme conditions, a 15C rate was also used. Discharge curves of the 2-mm cell with a 9-nm-thick SiO_2 electrolyte are presented in Fig. 3. Due to technical constraints originating from the use of a probe station for the measurements (as described in the Experimental Procedure section) the cells were charged to different levels of total charge. To compensate for this, the results of discharge tests consider the percentage of charge transferred back during discharge in the light of the absolute value of the charge received by the cell. The time period of charging was multiplied by the current value to calculate the actual charge passing between the electrodes. In discharge, the charge was estimated by multiplying the current by the time in which the voltage was positive. The amount of charge passed through the cell when charging and discharg-

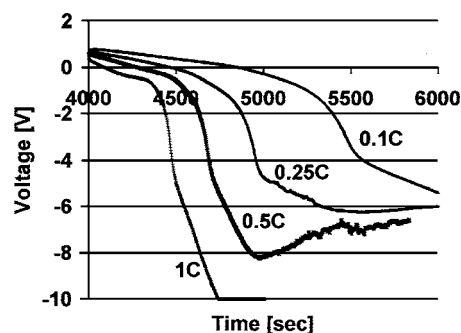


FIG. 3. Discharge plots of 2-mm cells with a 9-nm-thick SiO_2 electrolyte at different rates.

ing and the percentage of the reversible charge (discharge divided by charge) can be seen in Table I. The data shown in Fig. 3 and in Table I indicate that the ability to store and deliver charge is inversely proportional to current density. Figure 3 demonstrates this by the longer period of positive voltage during discharging and the higher voltage during discharging, and Table I shows that there is a higher percentage of charge retrieved when discharging at lower rates. This observation is characteristic to energy storage devices by charge transfer. Other studies of cycle testing involving Li_xCoO_2 also show higher capacities and higher voltage values at slower rates.^{7,18,22} Takano *et al.* speculated that at large current densities, due to diffusion limitations, lithium is plated on the surface of LiCoO_2 , resulting in a large voltage drop in a carbon- LiCoO_2 battery with a liquid electrolyte.²³ Similarly, for our cell high discharge rates might lead to the formation of nonequilibrium lithium-rich alloys of lithium and silicon closer to the $\text{SiO}_2/\text{polysilicon}$ interface, thereby causing stresses and large local concentration gradients and inhibiting further lithium diffusion.

Our top-contact geometry allows us to observe such phenomena at the lower contact region, where lateral conductivity is necessary. At increasing charge and discharge rates, we have noticed precipitates forming at the edges of the active area in this region on the surface of the polysilicon. Figure 4 shows SEM images of the polysilicon surface in the vicinity of the edge of the active area of three cells; one of them was not tested, one was tested at 0.5C, and the third was tested at the extreme rate of 15C. As can be seen from looking at the micrographs, testing at higher rates produced more precipitates and they appear closer to the edge of the active area. Those precipitates are believed to originate in the reaction between the lithium and silicon during charging. Figure 5 shows one of the precipitates at higher magnification (SEM).

TABLE I. Charge exchange in charging and discharging the 2-mm size 9-nm-thick oxide cell.

Rate	Charge in charging (C)	Charge in discharging (C)	Percentage of reversible charge (%)
0.1C	1.6×10^{-4}	3.39×10^{-5}	21.19
0.25C	4×10^{-4}	4.66×10^{-5}	11.65
0.5C	5.6×10^{-4}	5.4×10^{-5}	9.64
1C	1.2×10^{-3}	3.44×10^{-5}	2.86

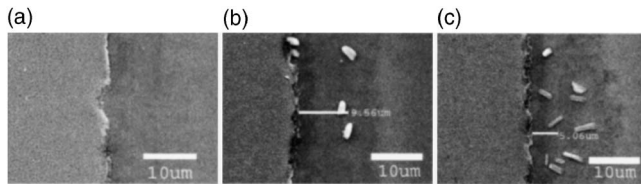


FIG. 4. SEM picture of the active area edge of three cells: (a) not tested, (b) tested at 0.5C, and (c) tested at 15C.

Lithium and silicon form four different compounds mentioned previously and the formation reaction involves a large volume change of more than, e.g., 200% (for the orthorhombic $\text{Li}_{12}\text{Si}_7$). During the charge process, lithium ions are transported to the polysilicon electrode where they receive an electron and react with silicon. At high charge rates it may be that the comparatively slow diffusion of lithium results in pockets of high lithium concentration in the polysilicon layer, leading to the nucleation and the eruption of the Li-Si precipitates to the surface at shorter distances from the active area edge. These precipitates do not dissolve upon discharging. This hypothesis is also supported by the low percentage of reversible charge measured and its dependence on the charging rate.

In order to model the complete set of capacitances and resistances in the structure and establish an electrical model of the device, impedance measurements were performed on cells with an active area of $2 \times 2 \text{ mm}^2$ and a 9-nm-thick electrolyte. An ac voltage signal of 100 mV was applied and the response current was measured at different frequencies. The high series resistance of our cells required us to set the value of the input voltage signal higher than is commonly done in impedance studies. Just the same, it was assumed that the current response current was linear and therefore at the same angular frequency. The complex plane representation of the measured values of impedance for one of the cells is shown in Fig. 6. The data represented by filled diamonds are the negative of the measured imaginary part of the impedance versus the real part at different frequencies.

On the basis of these data an equivalent circuit model of the cell was inferred and is presented in Fig. 7. A theoretical impedance curve based on this suggested equivalent circuit was calculated using ZVIEW, the results of which are presented in Fig. 6. Each component of the circuit consists of a capacitor or a constant phase element (CPE) connected in parallel with a resistor. In the complex plane of the electrical

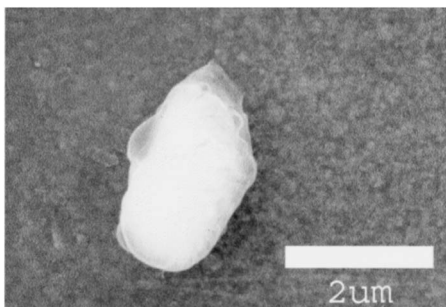


FIG. 5. SEM picture showing one of the precipitates at a higher magnification.

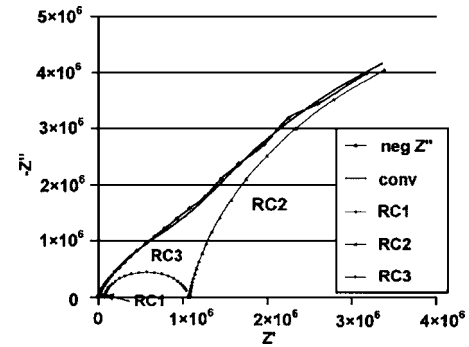


FIG. 6. A Cole-Cole plot of one of the 2-mm cells (9-nm-thick oxide) with three depressed semicircles composing the theoretical plot corresponding to an equivalent circuit.

signature of each such component is a semicircle. CPEs can describe a variety of physical features that have near-capacitor-like electrical signatures including inhomogeneity and roughness of the electrolyte/electrode interface. The impedance of a CPE is given by Eq. (2) where A is a frequency-independent constant and n is a constant between 0.5 and 1 (equal to 1 for a pure capacitor²⁴):

$$Z(\omega) = A(j\omega)^{-n}. \quad (2)$$

In our measurements the instant values of the electrical parameters were such that there was considerable convolution of the three semicircles, designated RC1, RC2, and RC3 in Fig. 7. However, it was possible to deconvolve the data into three separate features as shown in Fig. 6 which also shows the good agreement between the impedance calculated from the proposed equivalent circuit and the measured values. At the same time we recognize that it may be possible to devise a different equivalent circuit capable of representing

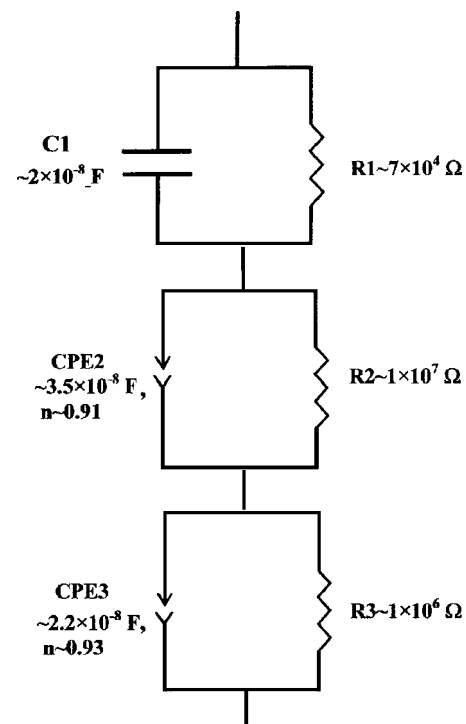


FIG. 7. The $\text{LiCoO}_2/\text{SiO}_2/\text{polysilicon}$ cell equivalent circuit based on impedance measurements.

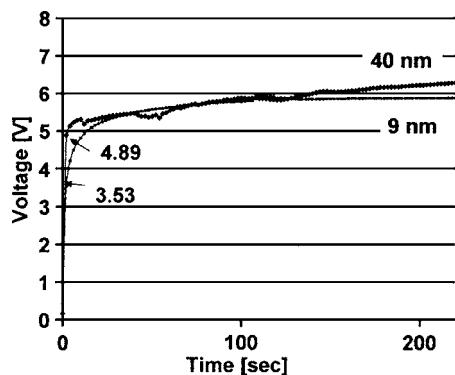


FIG. 8. Initial voltage increase in charging 2-mm cells with SiO₂ thicknesses of 9 and 40 nm.

the data we have taken. To discriminate between various equivalent circuits it is instructive to compare values of physical parameters that are derived from the fits to the various models. Although we cannot directly attribute the different current-impeding components in the suggested equivalent circuit to separate the cell's elements and processes, we can assume that the resistors in the circuit represent the electronic resistances of the electrodes, the ionic resistance of the electrolyte, the resistance of the mixed conducting electrode, as well as any kinetic barriers. The capacitors and CPEs in the circuit are representative of charge transfer across the electrolyte/electrode interfaces which include the capacitance induced by the polarization of the dielectric SiO₂ layer and its interfaces with the LiCoO₂ and polysilicon electrodes.

In order to identify some of the main components in the circuit model, we can estimate the electrolyte resistance from measurements made at different thicknesses assuming that the electrolyte series resistance is the largest component of the real part of impedance. The initial voltage increase in charging is a result of the IR drop and directly depends on the electrolyte thickness. The activation overpotential, i.e., due to kinetic barriers, can be minimized by charging at low rates. Shown in Fig. 8 are the cell response curves of two cells charged at 0.25C. With the exception of their oxide thickness values of 40 and 9 nm, the structures are otherwise identical. The initial voltage increase above 2.5 V (the expected open circuit voltage) for these structures can be used in conjunction with Eq. (1) to estimate the resistance of the cells with 40- and 9-nm-thick oxides to be 9.4×10^7 and $4.1 \times 10^7 \Omega$, respectively. The first value is higher than the theoretical equivalent circuit value given in Fig. 7 for R2; however, this still suggests that the major contribution to the cell resistance comes from the oxide layer. SiO₂ has a bulk resistivity of $\rho \sim 10^{15} \Omega \text{ cm}$,²⁵ and based on this value the resistance of a 9- and a 40-nm-thick SiO₂ can be roughly estimated as $\sim 9 \times 10^8$ and $4 \times 10^9 \Omega$, respectively. Those values are higher than the experimental result. We speculate that the origin of this difference lies in the thin-film nature of the oxide and the fact that it was grown via the thermal oxidation of polysilicon.

Similarly, we can independently calculate the capacitance of the electrolyte to compare to the equivalent circuit model. The capacitance C of the SiO₂ layer can be calculated as

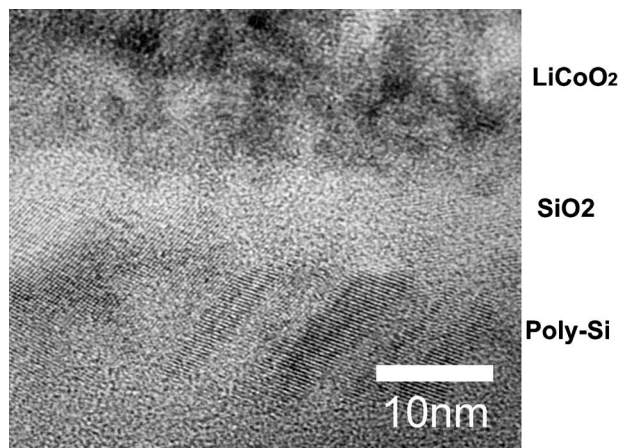


FIG. 9. A XHRTEM picture of the LiCoO₂/SiO₂/polysilicon layers with a 0–7-nm-thick SiO₂.

$$C = \frac{A\epsilon_0\epsilon}{d}, \quad (3)$$

where $A=4 \text{ mm}^2$ is the active area of the cell, $\epsilon=4$ is the relative dielectric constant of SiO₂, $d=9 \text{ nm}$ is the measured oxide thickness, and $\epsilon_0=8.85 \times 10^{-14} \text{ F/cm}$ is the permittivity of vacuum. Inserting these numbers results in a calculated capacitance value of $\sim 6.29 \times 10^{-8} \text{ F}$, which is comparable to the fitted values of the structure in Fig. 7. This value is, however, three orders of magnitude lower than the cell capacitance as shown in Fig. 3 and Table I, indicating that the majority of power was induced by electrochemical reactions and not by the oxide electronic capacitance. Based on the calculations described above, we can identify the second element of the circuit model in that figure, composed of R2 and CPE2, as representing the electrolyte in the cell. It is clear that the SiO₂ electrolyte, as modeled in this structure for this thickness, is the highest barrier to current flow in the cell. The other two elements can be reasonably attributed to the effects of interfaces and kinetic barriers of the reduction-oxidation reaction.

One of the most effective ways to decrease the series resistance of a battery and improve its performance would be to reduce the electrolyte thickness. However, an attempt at cell fabrication with a thinner SiO₂ layer resulted in the vast majority of the cells being shorted, thereby making their current-voltage behavior equivalent to that of a resistor. XHRTEM imaging revealed thickness variations in the ultra-thin SiO₂ that can be attributed to anisotropy in the oxidation rate of the polysilicon layer. A XHRTEM image showing the SiO₂ interfaces of the LiCoO₂/SiO₂/polysilicon structure can be seen in Fig. 9. The SiO₂ thickness ranges from 0–7 nm, leading to the creation of electronic shorting paths between the electrodes. The dielectric breakdown strength of SiO₂ is $\sim 10^7 \text{ V/cm}$.²⁵ The breakdown voltage of a 7-nm, high-quality thermal SiO₂ is therefore approximately 7 V. Furthermore, as 7 nm represents the thickest portion of the layer, the calculated breakdown voltage of 7 V represents an upper limit, and would therefore be much lower for thinner local areas of the oxide. Thus, the breakdown point of the SiO₂ is reached during our cell charging and discharging.

This breakdown results in a transition for the SiO₂ to an electronically conductive layer, thereby preventing it from functioning as the required electronically insulating electrolyte. SiO₂ is an interesting material for electrolyte applications; however, the series resistance to lithium-ion transport must be lowered to be technologically useful in a battery. To continue along this path of improving the electrolyte properties by lowering its thickness, an additional improvement in interfacial quality is required. Future work is needed to study interface reactions and to reduce roughness. An alternative path of improvement would be to alter the electrolyte structure, for example, by doping it with lithium containing salts.

SUMMARY AND CONCLUSIONS

We have demonstrated the exploitation of an ultrathin SiO₂ as a potential electrolyte in an integrated LiCoO₂/SiO₂/polysilicon solid-state thin-film lithium-ion power cell or controlled-ion-transport device. This work demonstrates that an electrically insulating electrolyte which is not initially doped with lithium is feasible if the electrolyte layer is extremely thin and uniform. Taking advantage of the microelectronics expertise of controlled and uniform thin films and high-quality interfaces has opened the door to alternative materials and improved properties of known materials for battery, electronic, and optoelectronic applications. Successful transport of lithium ions across the oxide is evident by the charging and discharging of our structures. All cells were fabricated and characterized using microelectronics-compatible processing and technology. The series resistance of the SiO₂ electrolyte is high, even at thickness values as low as 9 nm, thus limiting the discharge capacity. A reduction of the electrolyte thickness is limited by the anisotropy of the oxidation rate of the polysilicon granular surface, leading to creation of shorting paths in the electrolyte. Further reduction of the SiO₂ thickness may be accomplished by planarizing the polysilicon layer in order to create smoother interfaces between the electrodes and the electrolyte of the cells, as well as modifying the SiO₂ network for higher ion conductivity.

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